WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device, comprising:

a plurality of word lines;

a plurality of memory cells respectively selected by the plural word lines;

a plurality of bit lines to which the plural memory cells are connected respectively;

precharge circuits which respectively effect precharge operations on the plural bit lines upon non-selection of the plural word lines and stop the precharge operations when one word line is selected;

a plurality of first amplifier circuits which respectively include first MOSFETs of first conductivity type having gates connected to the plural bit lines and held in an off state under precharge voltages supplied to the bit lines by the precharge circuits and which are respectively brought to an operating state in response to select signals for selecting the bit lines to thereby amplify read signals on the bit lines; and

a first memory circuit including a second amplifier circuit including a plurality of second MOSFETs of second conductivity type, which have gates to which output signals of the plural first amplifier circuits are connected, and which are connected in parallel configurations and different from the first conductivity

type, said second amplifier circuit forming an amplified signal corresponding to signals outputted from the first amplifier circuits.

2. The semiconductor integrated circuit device according to claim 1,

wherein a memory current path of said each memory cell comprises a third and a fourth MOSFETs connected in a series configuration,

wherein a gate of the third MOSFET is supplied with a memory voltage retained in a latch circuit comprising two CMOS inverter circuits, and a gate of the fourth MOSFET is supplied with a signal for selecting a corresponding word line,

wherein the bit lines are read-only bit lines,

wherein the word lines are read-only word lines, and

wherein a pair of input/output nodes of the latch circuit is connected to a pair of write-only complementary bit lines through a pair of select MOSFETs switch-controlled by write-only word lines.

3. The semiconductor integrated circuit device according to claim 1, further including a fifth MOSFET having a source-drain path used as the memory current path of said each memory cell,

wherein whether the memory current path is formed

is determined according to the operation of selecting a corresponding word line.

4. The semiconductor integrated circuit device according to claim 2, wherein one second amplifier circuit is assigned to the plural first amplifier circuits, and the plural second amplifier circuits are provided, whereby read signals are outputted in plural bit units.

5. Th semiconductor integrated circuit device according to claim 3, wherein one second amplifier circuit is assigned to the plural first amplifier circuits, and the plural second amplifier circuits are provided, whereby read signals are outputted in plural bit units.

6. The semiconductor integrated circuit device according to claim 2, further including:

bit lines disposed in a direction opposite to the bit lines, bit line precharge circuits and a plurality of word lines, which are provided with respect to the first amplifier circuits; and

fifth MOSFETs of first conductivity type, which respectively have gates respectively connected to the bit lines disposed in the opposite direction and are respectively held in an off state under precharge

voltages supplied to the bit lines by the precharge circuits,

wherein the fifth MOSFETs are respectively connected in the form parallel with the third MOSFETs, and

wherein the word line corresponding to any one of the bit lines disposed on both sides of each of the first amplifier circuits is brought to a selected state.

7. The semiconductor integrated circuit device according to claim 2, wherein threshold voltages of the third and fourth MOSFETs are respectively formed as threshold voltages smaller than threshold voltages of MOSFETs constituting the CMOS inverter circuits.

8. The semiconductor integrated circuit device according to claim 2, further including a second memory circuit, which comprises:

a plurality of word lines;

a plurality of complementary bit lines;

memory circuits which are respectively provided at points wherein the plural word lines and the plural complementary bit lines respectively intersect and which comprise CMOS latch circuits; and

a plurality of memory cells which are respectively provided between pairs of input/output nodes of the memory circuits and the complementary bit lines and

comprise selection MOSFETs whose gates are connected to the word lines.

9. The semiconductor integrated circuit device according to claim 8, wherein the second memory circuit has an operation mode in which the second memory circuit is set to a low voltage in comparison with time upon a memory operation.

10. The semiconductor integrated circuit device according to claim 8, wherein the second memory circuit is formed so as to be larger than the first memory circuit in memory capacity.

11. The semiconductor integrated circuit device according to claim 2, further including a third memory circuit, which comprises:

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells comprising capacitors which are respectively provided at points where the word lines and the bit lines respectively intersect and which retain information charges therein, and selection MOSFETs respectively provided between information retention nodes of the capacitors and the bit lines and having gates connected to the word lines.

12. The semiconductor integrated circuit device according to claim 11, wherein the third memory circuit is formed so as to be larger than the first memory circuit in memory capacity.

13. A semiconductor device, comprising:

a plurality of word lines;

a plurality of bit lines;

a plurality of memory cells respectively connected to the plural word lines and the plural bit lines; and

amplifier circuits which are respectively connected to the plural bit lines and amplify potentials on the plural bit lines,

wherein each of the amplifier circuits includes a first MOS transistor of first conductivity type having a gate connected to one of the bit lines, and a second MOS transistor of second conductivity type having a gate connected to a source-drain path of the first MOS transistor.

14. The semiconductor device according to claim 13,

wherein the first conductivity type is a P type, and

wherein the second conductivity type is an N type.

15. The semiconductor device according to claim 13, further including precharge circuits which are

respectively connected to the plural bit lines and precharge the plural bit lines,

wherein each of the precharge circuits includes a third MOS transistor having a source-drain path connected between one of the plural bit lines and a power supply voltage.

16. The semiconductor device according to claim 15,

wherein each of the first MOS transistor and the third MOS transistor is a P channel type MOS transistor, and

wherein the second MOS transistor is an N channel type MOS transistor.

17. The semiconductor device according to claim 13, wherein the plural memory cells are respectively static memory cells.

18. A semiconductor device, comprising:

a plurality of first word lines;

a plurality of second word lines;

a first bit line;

a second bit line;

a plurality of first memory cells respectively connected to the plural first word lines and the first bit line;

a plurality of second memory cells respectively

connected to the plural second word lines and the second bit line; and

an amplifier circuit which is connected to the first and second bit lines and amplifies potentials on the first and second bit lines,

wherein the amplifier circuit includes a first MOS transistor of first conductivity type having a gate connected to the first bit line, a second MOS transistor of the first conductivity type having a gate connected to the second bit line, and a third MOS transistor of second conductivity type different from the first conductivity type,

wherein a drain of the first MOS transistor is connected to a drain of the second MOS transistor, and

wherein a gate of the third MOS transistor is connected to a drain of the first MOS transistor.

19. The semiconductor device according to claim 18,

wherein the first conductivity type is a P type, and

wherein the second conductivity type is an N type.

20. The semiconductor device according to claim 18, further including:

a first precharge circuit which is connected to the first bit line and precharges the first bit line; and

a second precharge circuit which is connected to

the second bit line and precharges the second bit line,

wherein the first precharge circuit includes a fourth MOS transistor having a source-drain path connected between the first bit line and a power supply voltage, and

wherein the second precharge circuit includes a fifth MOS transistor having a source-drain path connected between the second bit line and the power supply voltage.

21. The semiconductor device according to claim 20,

wherein each of the first, second, fourth and fifth MOS transistors is a P channel type MOS transistor, and

wherein the third MOS transistor is an N channel type MOS transistor.

22. The semiconductor device according to claim 18, wherein the plural memory cells are respectively static memory cells.

23. The semiconductor device according to claim 18,

wherein the first bit line and the second bit line extend in the same direction, and

wherein the amplifier circuit is formed in an area between a quadrangular area in which the plural first memory cells are formed and a quadrangular area in which the second memory cells are formed.

24. A semiconductor device formed on one semiconductor substrate, comprising:

a first word line;

a second word line;

a read bit line;

a first write bit line;

a first memory cell connected to the first and second word lines, the read bit line and the first write bit line;

a third word line;

a first bit line;

a second bit line; and

a second memory cell connected to the third word line, the first bit line and the second bit line,

wherein the first memory cell includes a first inverter circuit, a second inverter circuit having an input connected to an output of the first inverter circuit and an output connected to an input of the first inverter circuit, a first transistor having a source-drain path one of which is connected to the read bit line, a second transistor having a source-drain path connected to a first terminal, one of which is connected to the other of the source-drain path and the other of which is supplied with a first voltage, and a third transistor having a source-drain path one of which is connected to the input of the first inverter circuit and the other of which is connected to the first write bit line,

wherein a gate of the fist transistor is connected to the first word line,

wherein a gate of the second transistor is connected to the output of the first inverter circuit,

wherein a gate of the third transistor is connected to the second word line, and

wherein the second memory cell includes a third inverter circuit, a fourth inverter circuit having an input connected to an output of the third inverter circuit and an output connected to an input of the third inverter circuit, a fourth transistor having a source-drain path connected between the first bit line and the output of the third inverter circuit, and a gate connected to the third word line, and a fifth transistor having a source-drain path connected to the second bit line and the input of the third inverter circuit, and a gate connected to the third word line.

25. The semiconductor device according to claim 24, wherein the first voltage is a ground potential.

26. The semiconductor device according to claim 24, wherein each of the first through fourth inverter circuits includes one P type MOS transistor and one N type MOS transistor.

27. The semiconductor device according to claim 24,

wherein the first bit line and the second bit line are respectively bit lines commonly used for writing and reading,

wherein the first word line is a word line used for read only,

wherein the second word line is a word line used for write only, and

wherein the third word line is a word line commonly used in writing and reading.

28. The semiconductor device according to claim 24,

wherein the first memory cell is a multi-port memory cell,

wherein the second memory cell is a one-port memory cell,

wherein said semiconductor device includes a plurality of multi-port memory cells and a plurality of one-port memory cells, and

wherein the plural one-port memory cells are larger than the plural multi-port memory cells in memory capacity.

29. The semiconductor device according to claim 28, wherein the first memory cell is a two-port memory cell.

30. The semiconductor device according to claim 24, further including a second write bit line,

wherein the first memory cell further includes a sixth transistor having a source-drain path one of which is connected to the output of the first inverter circuit and the other of which is connected to the second write bit line, and a gate connected to the second word line.

31. A semiconductor device formed on one semiconductor substrate, comprising:

a first word line;

a second word line;

a read bit line;

a first write bit line;

a first memory cell connected to the first and second word lines, the read bit line and the first write bit line;

a third word line;

a first bit line;

a second bit line; and

a second memory cell connected to the third word line, and the first bit line and the second bit line,

wherein the first memory cell includes:

a latch circuit including a first inverter circuit, and a second inverter circuit having an input connected to an output of the first inverter circuit and an output connected to an input of the first inverter circuit;

a first and a second transistors whose

source-drain paths are series-connected between the read bit line and a first terminal supplied with a first voltage; and

a third transistor having a source-drain path connected between the latch circuit and the first write bit line and a gate connected to the second word line,

wherein a gate of the first transistor is connected to the first word line,

wherein a gate of the second transistor is connected to the latch circuit, and

wherein the second memory cell includes a third inverter circuit, a fourth inverter circuit having an input connected to an output of the third inverter circuit, and an output connected to an input of the third inverter circuit, a fourth transistor having a source-drain path connected to the first bit line and the output of the third inverter circuit, and a gate connected to the third word line, and a fifth transistor having a source-drain path connected to the second bit line and the input of the third inverter circuit, and a gate connected to the third word line.

32. The semiconductor device according to claim 31,

wherein one of the source-drain path of the first transistor is connected to the read bit line, and the source-drain path of the second transistor is connected

between the other of the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the input of the first inverter circuit and the first write bit line.

33. The semiconductor device according to claim 31,

wherein one of the source-drain path of the first transistor is connected to the read bit line,

wherein the source-drain path of the second transistor is connected between the other of the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the output of the first inverter circuit and the first write bit line.

34. The semiconductor device according to claim 31, wherein the first voltage is a ground potential.

35. The semiconductor device according to claim 31,

wherein each of the first through fourth inverter

circuits includes one P type MOS transistor and one N type MOS transistor.

36. The semiconductor device according to claim 31,

wherein the first bit line and the second bit line are respectively bit lines commonly used for writing and reading,

wherein the first word line is a word line used for read only,

wherein the second word line is a word line used for write only, and

wherein the third word line is a word line commonly used in writing and reading.

37. The semiconductor device according to claim 31,

wherein the first memory cell is a multi-port memory cell,

wherein the second memory cell is a one-port memory cell,

wherein said semiconductor device includes a plurality of multi-port memory cells and a plurality of one-port memory cells, and

wherein the plural one-port memory cells are larger than the plural multi-port memory cells in memory capacity.

38. The semiconductor device according to claim 37,

wherein the first memory cell is a two-port memory cell.

39. The semiconductor device according to claim 31, further including a second write bit line,

wherein the first memory cell further includes a sixth transistor having a source-drain path connected between the output of the first inverter circuit and the second write bit line, and a gate connected to the second word line,

wherein one of the source-drain path of the first transistor is connected to the read bit line,

wherein the source-drain path of the second transistor is connected between the other of the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the input of the first inverter circuit and the first write bit line.

40. A semiconductor device formed on one semiconductor substrate, comprising:

a plurality of multi-port memory cells and a plurality of one-port memory cells,

wherein the plural one-port memory cells are greater than the plural multi-port memory cells in memory

capacity.

41. The semiconductor device according to claim 40,

wherein the plural multi-port memory cells are respectively two-port memory cells,

wherein each of the plural multi-port memory cells is a static memory cell including 8 MOS transistors, and

wherein each of the plural one-port memory cells is static memory cell including 6 MOS transistors.

42. A semiconductor device formed on one semiconductor substrate, comprising:

a first word line;

a second word line;

a read bit line;

a first write bit line;

a first memory cell connected to the first and second word lines, the read bit line and the first write bit line;

a third word line;

a first bit line; and

a second memory cell connected to the third word line and the first bit line,

wherein the first memory cell includes:

a latch circuit including a first inverter circuit, and a second inverter circuit having an input connected to an output of the first inverter circuit and

an output connected to an input of the first inverter circuit;

a first and a second transistors whose source-drain paths are series-connected between the read bit line and a first terminal supplied with a first voltage; and

a third transistor having a source-drain path connected between the latch circuit and the first write bit line and a gate connected to the second word line,

wherein a gate of the first transistor is connected to the first word line,

wherein a gate of the second transistor is connected to the latch circuit, and

wherein the second memory cell includes a fourth transistor having a gate connected to the third word line and a source-drain path whose one is connected to the first bit line, and a capacitor having a pair of electrodes one of which is connected to the other of the source-drain path of the fourth transistor and the other of which is supplied with a second voltage.

43. The semiconductor device according to claim 42,

wherein one of the source-drain path of the first transistor is connected to the read bit line,

wherein the source-drain path of the second transistor is connected between the other of the source-

drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the input of the first inverter circuit and the first write bit line.

44. The semiconductor device according to claim 42,

wherein one of the source-drain path of the first transistor is connected to the read bit line,

wherein the source-drain path of the second transistor is connected between the other of the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the output of the first inverter circuit and the first write bit line.

45. The semiconductor device according to claim 42,

wherein the first voltage is a ground potential, and

wherein the second voltage is a plate potential larger than the ground potential.

46. The semiconductor device according to claim 42, wherein each of the first through fourth inverter circuits includes one P type MOS transistor and one N type MOS transistor.

47. The semiconductor device according to claim 42,

wherein the first bit line and the second bit line are respectively bit lines commonly used for writing and reading,

wherein the first word line is a word line used for read only,

wherein the second word line is a word line used for write only, and

wherein the third word line is a word line commonly used in writing and reading.

48. The semiconductor device according to claim 42,

wherein the first memory cell is a multi-port memory cell,

wherein the second memory cell is a one-port memory cell,

wherein said semiconductor device includes a plurality of multi-port memory cells and a plurality of one-port memory cells, and

wherein the plural one-port memory cells are larger than the plural multi-port memory cells in memory capacity.

49. The semiconductor device according to claim 48, wherein the first memory cell is a two-port memory cell.

50. The semiconductor device according to claim 42, further including a second write bit line,

wherein the first memory further includes a fifth transistor having a source-drain path on eof which is connected to the output of the inverter circuit and the other of which is connected to the second write bit line, and a gate connected to the second word line,

wherein the input of the first inverter circuit is connected to the output of the second inverter circuit,

wherein the output of the first inverter circuit is connected to the input of the first inverter circuit,

wherein one of the source-drain path of the first transistor is connected to the read bit line,

wherein the source-drain path of the second transistor is connected between the source-drain path of the first transistor and the first terminal,

wherein the gate of the second transistor is connected to the output of the first inverter circuit, and

wherein the source-drain path of the third transistor is connected between the output of the second inverter circuit and the first write bit line.

51. The semiconductor device according to claim 42, wherein the first through fourth transistors are respectively N channel type MOS transistors.